MULTI-KILOVOLT SOLID-STATE PICOSECOND SWITCH STUDIES*

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Abstract

Repetitive solid state picosecond switching is being developed for application to electromagnetic impulse sources. Low jitter and fast risetime are required to synchronize multiple modules of radiating array sources. While laser controlled photoconducting switches provide low jitter, they are expensive and have limited lifetime. We are studying an alternative technology using delayed avalanche breakdown semiconductor closing switches to drive arrays of impulse radiating antennas. The devices are rapidly pulse charged to enable low jitter picosecond switching. Single devices have demonstrated hold-off voltage exceeding 3 kV for silicon and 6 kV for silicon carbide. The silicon devices have demonstrated reliable operation at kilohertz repetition rates providing risetimes of approximately 100 ps.

I. SWITCH PHYSICS

The delayed breakdown diode (DBD) was discovered by I.V. Greckhov and A.F. Kardo-Sysoyev of the Ioffe Institute in St. Petersburg, Russia [1]. When certain silicon diode structures are rapidly pulsed beyond their static breakdown voltage, a delay of several nanoseconds is observed before a fast breakdown.

Delayed avalanche breakdown can occur when a reverse biased semiconductor junction is pulse charged so fast that the voltage across the junction exceeds the static breakdown voltage. The high field rise causes carrier motion and impact ionization in the bulk of the material. This leads to an ionization shockwave which moves across the bulk semi-conductor material with a speed exceeding the carrier drift velocity [2,3,4]. Delayed breakdown has been observed in various semiconductor structures, including PIN diode, bipolar transistor, and thyristor [2].

It is well established that picosecond delayed breakdown switching only occurs when the devices are over-volted on a time scale of a few nanoseconds or less [3,4,5].

II. DEVICE CHARACTERIZATION

A number of semiconductor device types were studied for picosecond pulse sharpening. In this short paper we limit discussion to two devices, but many other device types gave similar switching results. The first device was a silicon (Si) PIN diode with a static breakdown level of 1475 V. The second device was a silicon carbide (SiC) PIN diode with a static breakdown level of 1630 V.

We performed static measurements to determine the physical structure of the devices. The area of the diodes was determined by digitizing the image from an optical video microscope. The device capacity was measured as a function of reverse bias voltage, and the device current was measured as a function of forward and reverse bias voltage. Analysis of the capacitance as a function of reverse voltage gave the length L_N and impurity concentration N_V of the intristic region as shown in table 1. Forward IV curves indicated a series resistance of 0.1 Ω for the Si device and 14 Ω for the SiC device.

Table 1. Diode C-V data

Diode	Area (cm^2)	V_{PT} (V)	C_{PT} (pF)	L_n (μm)	N_V (cm^{-3})
Si#1	0.01	600	1.6	70	1.6 x 10^{14}
SiC#1	0.0075	600	5.4	12.9	4.1x 10^{15}

III. EXPERIMENTAL SETUP

Figure 1 shows a simplified circuit diagram of the pulse-line circuit which was used to characterize the silicon delayed breakdown devices. The nanosecond pulse from the 50 ohm source on the left was applied to reverse bias the diode junction.

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14. ABSTRACT
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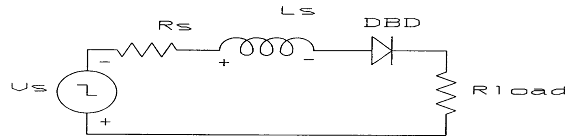

Figure 1. Simplified pulse shaper circuit used for delayed breakdown device testing

The pulse voltage doubles in amplitude, producing a high reverse voltage across the DBD. This occurs because initially the reverse biased diode appears as an open circuit. When the DBD switches, discharge current passes through the series combination of the dynamic switch impedance and the load resistance.

Figure 2 shows the instrumentation setup which was used to characterize the picosecond delayed breakdown phenomena occuring in the diodes. The picosecond shaper described in the previous paragraph contains the diode device under test. Coaxial delay cables were used on both the input and on the output to provide transit time isolation of the diode so that transmission line reflections did not disturb the measurement. The trigger pickoff synchronized the Tektronix model 11801 stroboscopic sampling digitizer with the nanosecond pulse charging waveform so that any time jitter in the switch closure can be observed on the digitizer. This configuration is referred to as external trigger.

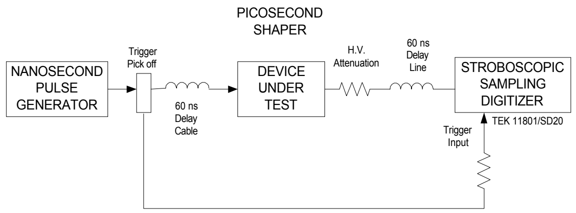

Figure 2. Block diagram of the instrumentation setup used to characterize the DBD test devices

IV. EXPERIMENTAL RESULTS

We record two waveforms, one with the diode shorted and the other with the diode in the circuit. We refer to these two waveforms as the "nanosecond driving pulse" and "sharpened output pulse". Figure 3 shows the two experimentally measured waveforms for the silicon device. The slow rising (dashed line) waveform is the pulse charging waveform from the nanosecond pulser, while the fast rising (solid line) waveform is the output voltage from the diode shaper. For both waveforms the digitizer was externally triggered from the nanosecond generator. The two waveforms are thus time correlated, and it can be seen that the DBD device breaks down near the peak voltage on the pulse charging waveform and closes rapidly. The nanosecond pulse charging waveform has a low level prepulse, followed by a region of slow rise, and finally a region of fast rise. The DBD switch was effective at blocking the prepulse and slow rise and breaking down rapidly near peak voltage. This is the desired behavior for a pulse sharpening device.

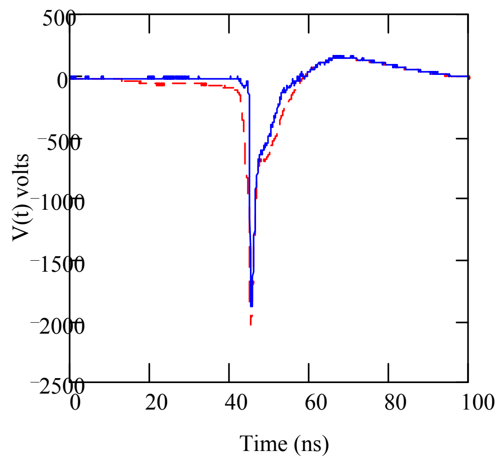

Figure 3. Measured voltage waveforms show nanosecond driving pulse (dashed line) and sharpened output pulse (solid line).

Figure 4 shows the output waveform at a finer time resolution. The sharpened pulse displays a risetime of 126 ps to a 2.1 kV peak voltage. This is to be compared with the pulse charging waveform which had a risetime of 2 ns. The risetime is seen to be decreased by an order of magnitude with minimal loss in peak voltage. Time jitter with respect to the driving pulse was below 25 ps RMS.

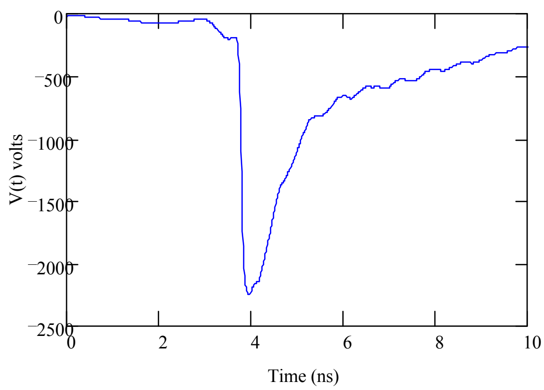

Figure 4. Sharpened output pulse for Si device showing 126 ps risetime to 2.1 kV

The picosecond pulser will be used with an ultra-wideband impulse radiating antenna. The antenna radiates an electric field waveform which approximates the time derivative of the driving voltage pulse. Figure 5 shows the time derivative of the measured DBD shaper voltage waveform which peaks at 17 kV/ns.

Experiments were also performed with SiC devices. The SiC device package required operation with the cathode grounded as shown by figure 6. To provide the higher breakdown voltage for the SiC device, we used a single shot pulser. A low bandwidth single shot digitizer with a 0.8 ns risetime was used to observe the waveforms for the SiC device.

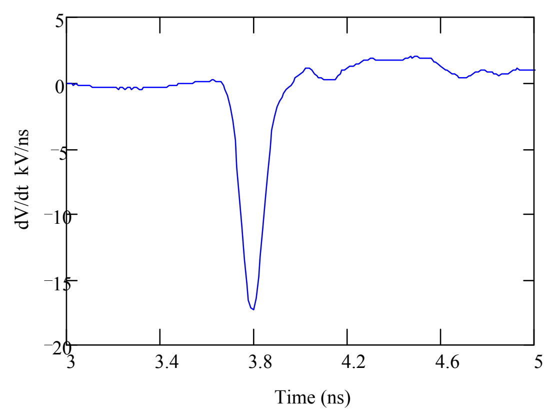

Figure 5. Derivative of the sharpened pulse

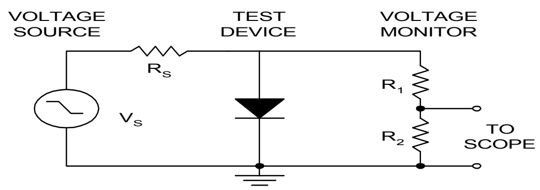

Figure 6. Simplified SiC avalanche diode test setup

Figure 7 shows the nanosecond driving pulse and the delayed avalanche breakdown of the SiC device. The driving pulse was observed by removing the device from the circuit. The data indicate pulse breakdown at 5.7 kV with a fast drop to a residual level of 1.7 kV. The bulk of the residual voltage is due to ohmic drop in the 14 Ω series resistance. The peak device current was 90 A which gives a current density of 12 kA/cm^2. The SiC device was pulsed hundreds of times with no observible degradation.

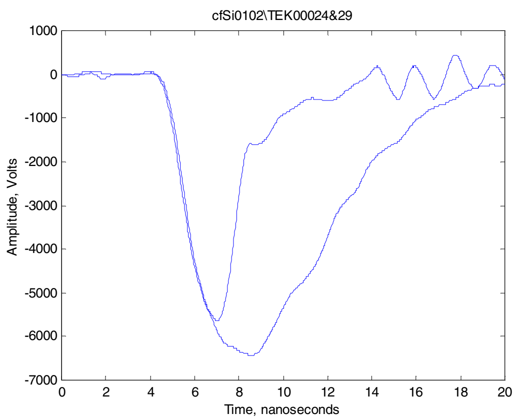

Figure 7. Measured waveforms showing nanosecond driving pulse and subnanosecond delayed avalanche dreakdown of SiC device

The observed risetime was instrument limited. The single shot data indicates subnanosecond delayed avalanche breakdown for SiC but does not allow a determination of the ultimate switching speed or device lifetime in repetitive applications.

V. NUMERICAL SIMULATIONS

Numerical simulations were performed using the SILVACO device physics code to better understand the delayed avalanche breakdown phenomenon for both Si and SiC. The SILVACO code is commonly used in the industry for designing semiconductor devices and integrated circuits.

The current and voltage for the numerically modeled device relies on a solution of Poisson's equation and the continuity equations for electrons and holes. Secondary equations are used to specify particular physical models for the current densities, generation rates, and recombination rates. The charge transport model is obtained by applying approximations and simplifications to the Boltzmann transport equation. The model used in the simulations performed in this paper is the simplest and is known as the "drift-diffusion" model.

Figure 8 shows the 0.008 cm^2 PIN diode structure which was simulated for the 75 μm length Si device with impurity density of 10^{14} cm^{-3} in the intristic region. A Gaussian driving pulse waveform was chosen to approximate the driving pulse used in the experiment.

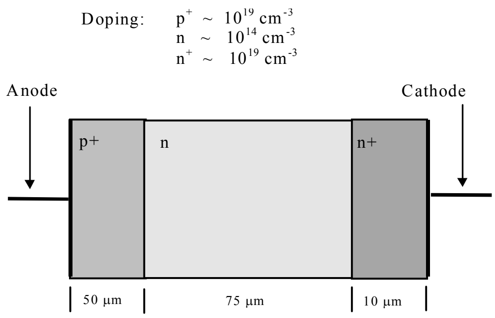

Figure 8. Si diode structure used in the simulations

Figure 9 shows the Gaussian driving pulse, the simulated diode voltage, and voltage across the 50 ohm load. Note that polarities are inverted relative to experimental data of figures 3 and 4. The load voltage waveform shows a prepulse feature due to displacement current in the dynamic junction capacity followed by a rapid rise. Figure 10 shows the load voltage waveform in more detail. The code predicts a transition time of 113 ps from the 700 V prepulse level to a peak amplitude of 2300 V with dV/dt of 17 kV/ns. Simulations were also performed for multiple series connected devices. Simulation of two Si devices driving a 100 Ω load predicted a transition time of 107 ps to 4.6 kV. Simulation of four Si devices driving a 200 Ω load predicted a transition time of 97 ps to 9.0 kV with dV/dt of 70 kV/ns.

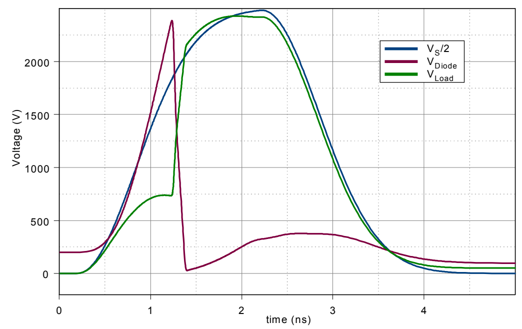

Figure 9. Simulation result showing matched driving voltage, the diode voltage, and the load voltage for a single 75 μm Si device

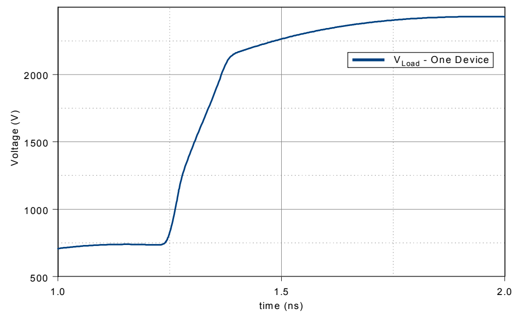

Figure 10. Simulation predicts risetime of 113 ps to 2.3 kV for 75 μm delayed breakdown Si sharpening switch

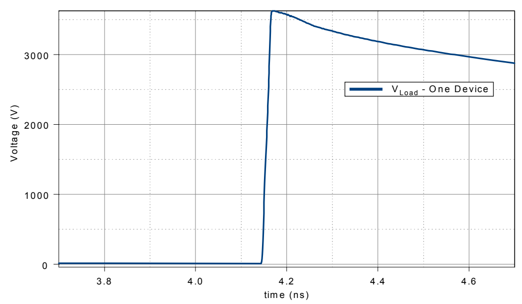

Figure 11. Simulation predicts risetime of 19 ps to 3.6 kV for 25 μm delayed breakdown SiC sharpening switch

Simulations were also performed for SiC devices. Figure 11 shows the simulated voltage waveform for a 0.001 cm^2 area 25 μm length SiC device with an impurity density of 8 X 10^{14} cm^{-3} driving a 50 Ω load. The prepulse level is insignificant, and the risetime is 19 ps to a peak voltage to 3.6 kV. Simulations of SiC devices with thicker intristic region and multiple series connected devices showed that the load voltage increases with thickness and number of devices. For example, figure 12 shows a simulation of the 12 kV voltage across a 100 Ω load delivered by two series connected 50 μm devices.

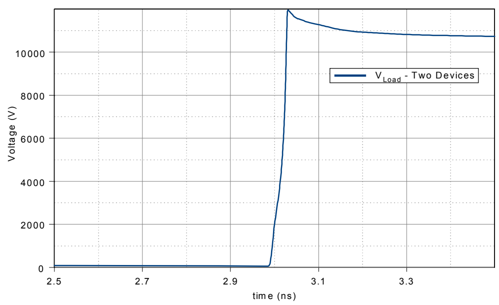

Figure 12. Simulation predicts risetime of 32 ps to 12 kV for two series connected 50 μm delayed breakdown SiC sharpening switches

VI. DISCUSSION

Experimental and theoretical study of delayed avalanche breakdown switching indicates that the switches can provide the performance required for driving the solid state switched array impulse source. Single switches were demonstrated to hold-off 3 kV for Si and 6 kV for SiC devices. In previous work we have demonstrated pulsers employing series connection of 18 low voltage devices [6]. The incorporation of the high voltage switches into similar circuits should allow picosecond pulse generation at the level of tens of kilovolts which will enable powerful radiating impulse sources and other applications.

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